Assignee: Intel Corporation

IN THE SPECIFICATION

Please amend the "Related Applications" paragraph 1 to now read:

[0001] This application is a continuation of Serial No. 09/894,638 filed on June 27, 2001, entitled "CACHE ARCHITECTURE WITH REDUNDANT SUB ~~ARRAY."~~ ARRAY", which issued December 9, 2003 as U.S Patent No. 6,662,271. This application is related to Serial No. 09/893,779 filed on June 27, 2001, entitled "ON-DIE CACHE MEMORY WITH REPEATERS" and Serial No. 09/894,513 filed on June 27, 2001, entitled "CACHE ARCHITECTURE FOR PIPELINED OPERATION WITH ON-DIE PROCESSOR", both of which are assigned to the assignee of the present application.